## AMENDMENTS TO THE SPECIFICATION

1. Please substitute paragraph 0004 as follows:

5        "Recently, semiconductor devices have been integrated so highly that integrated semiconductor devices have been designed on a nanometer level instead of a micron level (e.g., The National Technology Roadmap for Semiconductors Technology Needs, SIA, 2001 edition). In accordance with the SIA roadmap, by_2002, scaling of a sub-100nm device will need a gate oxide thickness ($t_{ox}$) in the range of about 12 to 15

10       angstroms. However, this raises a thorny problem of how to evaluate quality of an ultra-thin gate oxide layer with a thickness of 10 to 20 angstroms in terms of interface traps ($N_{it}$)."

2. Please substitute paragraph 0011 as follows:

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         "The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

20       Fig.1 (a) schematically shows_the fixed-based level pumping (CP) setup."

3. Please substitute paragraph 0022 as follows:

         "The present invention is directed to a method for accurately determining

25       interface traps (hereinafter referred to as $N_{it}$) in a semiconductor/oxide interface of advanced metal-oxide-semiconductor (MOS) devices having a short channel length and an ultra-thin gate oxide thereof. The MOS devices_to be tested_are fabricated by state-of-the-art integrated circuit (IC) manufacturing techniques. For example, a high-quality ultra-thin gate oxide layer having a thickness of about 12Å to 16Å (direct

30       tunneling regime) is formed on a cleaned surface of a semiconductor substrate by using a known Rapid Thermal Nitric Oxide (RTNO) process. In some cases, a Remote Plasma Nitridation (RPN) treatment is then used after the gate oxide formation for

reducing_the gate current leakage by a scale of about 2 to 3 orders. The masked lengths ranging from 0.22. m to 0.11. m are used."

4. Please substitute paragraph 0031 as follows:

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"(1) High-low frequency CP method: First, ~~the $I_{CP}$'s~~ the $I_{CP}$ currents for various frequencies are measured as shown in Fig.6. At a low gate pulse frequency, for example, $10^4$ Hz, the group-2 curve (curve (2)) is considered as the leakage current. Curve (1) is the measured $I_{CP}$ at a high gate pulse frequency, for example, 1MHz. A

10    correct $I_{CP}$ (group-3 curve) is obtained by subtracting curve (2) from curve (1)."

5. Please substitute paragraph 0032 as follows:

"(2) Incremental frequency CP method: From the measured $I_{CP}$ for various

15    frequencies, the difference of $I_{CP}$ between two successive frequencies is taken as shown in Fig.7. For example, $I_{CP\,(1MHz)}$-$I_{CP\,(500kHz)}$ is regarded as the $I_{CP}$ at 500kHz since $I_{CP}$ is directly proportional to_f."

20    6. Please substitute paragraph 0038 as follows:

"In summary, this invention provides a new CP methodology that is demonstrated for ultra-short channel length and ultra-thin gate oxide in the range 12Å to 16Å. It allows fast and easy calculation of the $N_{it}$ generated during the process. This

25    method is superior to the conventional CV method for $N_{it}$_characterization in that the latter needs a large area capacitor samples. On the other hand, both the Incremental frequency CP method and the High-low frequency CP method can be applied to evaluate the hot carrier reliability in terms of the interface traps for deep sub-micron scale devices. The proposed method not only can be used to calculate the $N_{it}$ values

30    but also be useful as a monitor of the oxide quality in an ultra-thin gate oxide process."

7. Please delete Table 1 in page 6, paragraph 0038. A legible Table 1 is respectfully submitted in this Amendment. No new matter is introduced in the newly submitted Table 1 and the Applicants wish to make the newly submitted Table 1 printed in a

5 separated paper a part of drawings (Fig.10) for the sake of clarity.

8. Please add the description of FIG.10 (Table 1) in "BRIEF DESCRIPTION OF THE DRAWINGS" section of the specification:

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"FIG.10 illustrates Table 1 that shows the relating equations for determining the interface traps, $N_{it}$ that can be calculated from the $I_{CP, MAX}$."

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